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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,174	03/10/2004	Udayakumar Cholleti	SUNMP399	5131

32291 7590 05/16/2006

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EXAMINER	
THOMAS, SHANE M	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,174	CHOLLETI ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the application filed 3/10/2004. Claims 1-22 are presented for examination and are currently pending.

In the response to this Office action, the Examiner politely requests that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line numbers in the specification and/or drawing figure(s). This will assist the Examiner in prosecuting this application.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of [column # / lines A-B] to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as "[2/1-6]."

Specification

The disclosure is objected to because of the following informalities:

In the Cross Reference section of the disclosure, the Attorney Docket number should be removed and the serial number 10/798742 entered in its place.

Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 3,4, and 11 are objected to because of the following informalities:

As per claim 3, the term --information-- is redundant and repeated twice.

As per claim 5, the term --references-- should be corrected to --reference-- since both the table and the structure perform the --referencing--.

As per claim 11, the term --is-- should be corrected to --are-- as both the table and the mapping framework reference.

Claim 4 is objected to as being dependent upon an objected claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Arndt et al. (U.S. Patent No. 6,931,471).

As per claim 1, Arndt teaches a **first page and a second page in a memory** (which the Examiner is considering to be a combination of physical memory 110 and the entries of the cached TCE table that are stored in the logic 150 [4/35-36]; such an interpretation is in light with

scope of the invention of the Applicant as the Applicant teaches that --the memory-- 120 comprises the physical addresses space, a control table, a page mapping structure, and a translation table), **the first page containing data capable of being copied to the second page** [3/59-4/11], **a table** (element of the logic 150 that caches the copies of the TCE entries - 4/35-36]) **in the memory** (as defined) **identifying the first page and the second page** (via virtual to physical mapping as shown in figures 2 and 3 of Arndt). The **table is capable of being enabled and disabled for access to the first page and the second page** [5/4-15]. The --table-- is disabled by restricting its access by the particular I/O device(s) enacted by the logic 150 through means of temporarily withholding permission for communication between the I/O adapters and the I/O bus, as the I/O device usually accesses the I/O bus 180 thereby accessing the TCE entry of the --table-- that maps the virtual page the physical page [4/29-36].

A structure (firmware 165) **coupled to the table** (as shown in figure 1), **the structure being capable of identifying data in the first page and the second page** (via mapping the virtual address to a physical address of the requested data as shown in figures 2 and 3), **wherein a device** (135, 140, or 145) **coupled to the memory** (via logic 150 - figure 1) **is capable of registering information in the structure** (entries 210-230 are linked to a respective I/O device - [4/50-56]) **before accessing the first page** (this is taught by Arndt since the virtual to physical mapping translation is set before an access to the physical page occurs - [5/29-41]).

As per claim 2, Arndt teaches **the structure containing information identifying the device** (entries 210-230 of the TCE 175, which is part of the structure 165, store information which identify the devices 135-145) - [4/50-56].

As per claim 3, Arndt teaches **the structure further including a record** (210-230) **to store the information**. Each of the records are linked to the devices 135-145.

As per claim 4, the **information is used to enable and disable access to the first and second pages** since the respective information in the records 210-230 are checked by the hypervisor 170 when determining which devices may use a first page that is to be copied to the second page [4/50-5/15].

As per claim 5, **the table and the structure reference a physical and virtual address** as shown in the entries of figures 2 and 3. The table, as discussed above, stores cached entries of the TCE 175, thus the table also references physical and virtual addresses.

As per claim 6, **the table is capable of storing the information** as the table stores cached copies of the TCE entries, which link devices to their particular physical pages it may use.

As per claim 7, **the device is capable of transmitting request for memory via direct memory access (DMA)** as taught in [1/36-39], [2/11-16], and [5/16-26].

As per claim 8, **the information in the structure is a record of the request for memory access to the first page** as a request to access data on a page requires a virtual to physical mapping between a virtual page 152 as used by the devices. Conversely, if a device did not request a data access to a first page, then a translation entry (information) would not have been present in the TCE table 175 for that particular device, as taught by the example in [5/10-14].

As per claim 9, Arndt teaches **a table** (element of the logic 150 that caches the copies of the TCE entries - 4/35-36]) **identifying a first page and a second page** (as the table caches

entries of the TCE table 175 [4/35-36], which identifies a first and second pages as shown in figures 2 and 3), **a mapping framework** 165 **coupled to the table** (as shown in figure 1) **identifying the first and second page** (as shown in figures 2 and 3), and **a record** (210-230) **in the mapping framework capable of storing information identifying a device** (as records 210-230 are linked to a respective I/O device 135-145 [4/50-56]) **before storing data in the first and second page** (the virtual to physical mapping structure is set before an access to the physical page occurs - [5/29-41]).

As per claim 10, it can be seen by Arndt that **the first page and the second page each have a unique physical address** as the first and second pages each are physical pages as shown in reference to figure 2 and 3. Further it is well known in the art that different physical pages have unique physical memory addresses.

As per claim 11, **the table and the mapping framework are capable of referencing the unique physical addresses and a virtual addresses** as both the table and framework comprise entries that contain virtual and physical pages. Refer to the discussion of claim 5, supra.

As per claim 12, **the device uses DMA to access the first and second pages** as taught in [1/36-39], [2/11-16], and [5/16-26].

As per claim 13, **the record identifies the first page and the second page** (i.e. the "source" page and the "destination" page) as shown in figures 2 and 3. For example the record 210 of figure 2 shows physical page 115.3 (i.e. first page) in entry 210.4, and once the copying takes place, shows physical page 115.5 (second page).

As per claim 14, the first and second pages are part of physical memory 110, which is a physical addresses space - [3/6-12].

As per claim 15, Arndt teaches **disabling access to a page in a memory** [5/4-15], **copying the page in the memory** [5/27-30], **wherein the page is identified by a structure** 175 (via virtual to physical page mapping) **coupled to a table** (element of the logic 150 that caches the copies of the TCE entries - 4/35-36] and coupled to the structure 175 as shown in figure 1) **in the memory** (wherein the memory comprises a combination of physical memory 110 and the entries of the cached TCE table that are stored in the logic 150 [4/35-36], as discussed with claim 1, supra), **the structure being capable of storing information identifying a device** (135-145), which is done by entries 213-230 (figures 2 and 3) - [4/50-56], and **enabling access to the page in memory** [5/30-41].

As per claim 16, **a first access to the page is registered in the structure** as a memory access to the page does not occur until the virtual to physical translation is set before an access to the physical page can occur - [5/29-41]).

As per claim 17, Arndt teaches **storing information transmitted by the device in a record in the structure** as the device transmits a request to access a particular virtual page, which is then stored in structure to map the virtual page to a physical page. In other words the request from the device is stored as information in the structure in order to link that device to that particular used page in physical memory 110, and used when moving data from one page in memory to another as discussed previously and throughout Arndt. Refer to [4/50-56].

As per claim 18, **disabling access to the page in a memory includes disabling device memory access** [5/4-14].

As per claim 19, **enabling access to the page further includes enabling device memory access** [5/35-39].

As per claim 20, **copying the page includes updating a record in the structure** as shown in figure 3 (entry 4 of records 210 and 230 is shown as being updated to reflect physical page 5) and taught in [5/29-34].

As per claim 21, **storing information identifying a device further includes accessing a pre-relocation method** as Arndt teaches using the information that identifies which devices are linked to particular pages that will be part of the page copying process in [4/50-56]. The pre-relocation process is taught by Arndt as comprising a routine run by the hyperviser 170 as assessing which devices are linked to the page that is to be unmapped [4/65 - 5/14].

As per claim 22, **storing information identifying a device further includes permitting access via DMA** as taught by Arndt in 1/36-39], [2/11-16], and [5/16-26]. In other words, once a device's virtual pages to access have been mapped to the proper physical pages, the I/O device may use DMA to access those pages of physical memory.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Boettner et al. (U.S. Patent No. 4,777,589) teaches linking an I/O device register with two pages of real memory with access IDs (figure 5).

Beukema et al. (U.S. Patent Application Publication No. 2002/0091841) teaches a network device that uses remote DMA to access a system's physical memory pages and regulates accesses to the physical memory pages on a node-to-node basis.

Elnozahy et al. (U.S. Patent Application Publication No. 2005/018496) teaches new page mapping and coalescing pages.

Willman et al. (U.S. Patent No. 6,986,006) teaches restricting DMA access to memory pages from I/O on a device-by-device basis [9/16-42].

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

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